

Appl. No. 10/607,911
Amdt. Dated: July 13, 2005
Reply to Office Action of
April 29, 2005

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) An integrated PCI interface card used in a bus system including a PCI host controller, comprising:

at least two bus masters;

a control unit electrically connected to the at least two bus masters for generating controlling transmissions of bus request signals to the PCI host controller and bus acknowledge signals of to the two bus masters; and

a multiplexer for selecting an unused address to act as an identification selection signal of one of the at least two bus masters; and

an EEPROM electrically connected to the multiplexer for assigning an initial identification selection signal to one of the at least two bus masters at power start-up and recording the unused address after power start-up.
2. (Original) The integrated PCI interface card of Claim 1, wherein the at least two bus masters share a same interrupt control signal.
3. (Cancelled)
4. (Original) An integrated PCI bus system, comprising:

at least one integrated PCI interface card as recited in Claim 1;

a PCI host controller for arbitrating which PCI interface card owns use permission;

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at least one bus request signal issued by the at least one integrated PCI interface card to the PCI host controller;

at least one bus acknowledge signal issued by the PCI host controller to the at least one integrated PCI interface card for replying the at least one bus request signal; and

at least one identification selection signal issued by the PCI host controller for selecting one bus master of the integrated PCI interface card.

5. (Original) The integrated PCI bus system of Claim 4, further comprising at least one PCI interface card having a single bus master.

6. (Original) The integrated PCI bus system of Claim 4, wherein the at least two bus masters of the integrated PCI interface card share a same interrupt control signal.

7. (Original) The integrated PCI bus system of Claim 4, wherein the PCI host controller assigns an unused address as another identification selection signal of the integrated PCI interface card by means of using a software program to scan unused address lines after power start-up.

8. (Original) The integrated PCI bus system of Claim 4, wherein the at least two bus masters of the integrated PCI interface card own a use permission in a rotating turn.

9. (New) An integrated PCI bus system, comprising:

at least one integrated PCI interface card as recited in Claim 1;

a PCI host controller for arbitrating which PCI interface card owns use permission, wherein the PCI host controller assigns an unused address as another identification selection signal of the integrated PCI interface card by means of using a software program to scan unused address lines after power start-up;

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at least one bus request signal issued by the at least one integrated PCI interface card to the PCI host controller;

at least one bus acknowledge signal issued by the PCI host controller to the at least one integrated PCI interface card for replying the at least one bus request signal; and

at least one identification selection signal issued by the PCI host controller for selecting one bus master of the integrated PCI interface card.